REMARKS

Claims 1-12 and 22-24 are currently pending. Claims 1-12 and 22-24 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,005,812 (Mullarkey) in view of U.S. Patent No. 5,796,285 (Drouot) and U.S. Patent No. 6,249,473 (Lau).

Please add new Claim 25 as set forth herein. No new matter has been added.

Regarding the rejection of independent Claims 1 and 23 under 35 U.S.C. §103(a), the Examiner states that the combination of Mullarkey in view of Drouot and Lau teache each and every limitation of the claims.

Claims 1 and 23 recite, in part, "an AND gate receiving said power control signal and clock control signal and outputting a control signal; a first transistor connected to the AND gate and controlled by said control signal; a second transistor and a third transistor connected in series, the series connected at one end to a voltage source and to the other end to the first transistor for generating a reference voltage". This combination of elements in their specific connection are neither taught nor disclosed by the cited references. For example, Claims 1 and 23 recite a first transistor connected to the AND gate and controlled by said control signal, and a second transistor and a third transistor connected in series, the series connected at one end to a voltage source and to the other end to the first transistor for generating a reference voltage. Lau et al. shows a NAND gate and an inverter, which is not an AND gate. Further, Drouot shows transistors 11-14 and transistors 15, 16 and 19 and a hysteresis comparator containing transistors 22-27 to generate its enable signal, which cannot be equated with the three transistors of Claims 1 or 23.

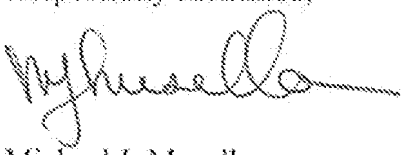
Accordingly, for at least the above-stated reasons, it is respectfully requested that the rejection of Claims 1 and 23 under 35 U.S.C. §103(a) be withdrawn.

New Claim 25 recites, in part, "a power control unit for determining a performance mode of the SOC and disabling the local DC voltage generators according to the performance mode, wherein a separate enabling clock signal is supplied to each DC voltage generator and the at least one unit of the plurality of subsystems associated each DC voltage generator." It is respectfully submitted that the cited references do not teach or disclose at least these features of Claim 25.

Independent Claims 1 and 23 are believed to be in condition for allowance. Without conceding the patentability per se of dependent Claims 2-12, 22, and 24, these are likewise believed to be allowable by virtue of their dependence on their respective amended independent claims. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims -12, 22, and 24 is respectfully requested.

Accordingly, all of the claims pending in the Application, namely, Claims 1-12 and 22-25, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



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